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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,084	06/22/2001	Vinson Dong	MR1115-310	4853

4586 7590 04/01/2005

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,084	DONG, VINSON	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 09/886084 Attorney's Docket #: MR1115-310
Filing Date: 6/22/2001;

Applicant: Dong

Examiner: Alexander Williams

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Initially, and with respect to the claim, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

In the claim rejected under 35 U.S.C. § 103(a) as being unpatentable over Eguchi et al. (U.S. Patent # 6,627,997 B1).

In the claim, Eguchi et al. (figures 1 to 11E) specifically figure show a naked chip motherboard module, comprising a motherboard **3**, said motherboard being a printed circuit board, on the motherboard having several regional spaces, each regional space having an accommodating chamber (within 4) to accommodate a chip, with connecting pins for the chip **6** in each regional space, so that after each chip is recorded and each

regional space is cut and separated, a plurality of chip 1 modules can be obtained for direct connection with circuit boards as required.

(15) The present invention, in a first aspect thereof, resides in a semiconductor module having a structure wherein a plurality of bare or packaged semiconductor chips are mounted on a single wiring board and a single heat spread plate is disposed on the plural semiconductor chips, characterized in that resin is filled around the plural semiconductor chips thus sandwiched between the wiring board and the heat spread plate and that adjacent semiconductor chips are connected together through the resin.

(16) As methods for mounting a bare or packaged semiconductor chip onto a wiring board there are a method wherein the semiconductor chip is mounted while a circuit-formed side of the chip faces down and is opposed to the wiring board, and a method wherein the circuit-formed side of the chip faces up and a circuit-free side of the chip is opposed to the wiring board. In a semiconductor module of a face-down bonding type wherein a semiconductor chip is connected to a wiring board while a circuit-formed side of the semiconductor chip faces down, pads formed on the circuit-formed side of the chip and pads formed on the wiring board are connected together through metal bumps. On the other hand, in a semiconductor module of a face-up bonding type wherein a semiconductor chip is mounted on a wiring board while a circuit-formed side of the chip faces up, a circuit-free side of the semiconductor chip is bonded to the wiring board using an adhesive, and pads formed on the circuit-formed side of the semiconductor chip and pads formed on the wiring board are bonded together with metal wires. The term "pads" as used herein indicate input-output terminals, which are sometimes called electrodes, electrode terminals, or simply terminals.

(17) The present invention, in a second aspect thereof, resides in a semiconductor module having a structure wherein a plurality of either bare semiconductor chips or packaged semiconductor chips are connected to a single wiring board electrically through metal bumps while circuit-formed sides of the chips face down, and a single heat spread plate is disposed above circuit-free sides of the chips, characterized in that a resin is filled between the wiring board and the semiconductor

chips, also between the semiconductor chips and the heat spread plate, and further between adjacent semiconductor chips, so that the semiconductor chips and the heat spread plate are bonded together with the resin, and the semiconductor chips are interconnected through the resin.

(18) The present invention, in a third aspect thereof, resides in a semiconductor module having a structure wherein circuit-free sides of a plurality of bare or packaged semiconductor chips are bonded to a single wiring board, a single heat spread plate is disposed on circuit-formed sides of the semiconductor chips, and pads formed on the circuit-formed sides and pads formed on the wiring board are bonded together with metal wires, characterized in that resin is filled between the semiconductor chips and the heat spread plate and also between the plural semiconductor chips, so that the semiconductor chips and the heat spread plates are bonded together with the resin, and the semiconductor chips are interconnected through the resin.

(19) In fabricating the semiconductor module according to the present invention, the semiconductor chips and the heat spread plate may be bonded together using a thermally conductive adhesive. In the semiconductor module of the type wherein semiconductor chips are metal wire-bonded to a wiring board while their circuit-formed sides face up, a spacer may be disposed between the heat spread plate and the semiconductor chips or between the heat spread plate and the wiring board to prevent metal wires from being crushed by the heat spread plate.

(20) The present invention, in a further aspect thereof, resides in a semiconductor module having a structure wherein a plurality of bare or packaged semiconductor chips are mounted on a single wiring board and a single heat spread plate is disposed on upper surfaces of the plural semiconductor chips, characterized in that an adhesive layer is present between the semiconductor chips and the heat spread plate, that resin is filled around the semiconductor chips sandwiched between the wiring board and the heat spread plate, and that the semiconductor chips are interconnected through the resin.

(21) The present invention, in a still further aspect thereof, resides in a semiconductor module having a structure wherein a plurality of bare or packaged semiconductor chips are mounted on a wiring board while circuit-formed sides thereof face up the

semiconductor chips and the wiring board are metal wire-bonded to each other, and a single heat spread plate is disposed on the circuit-formed sides of the plural semiconductor chips, characterized in that a metal wire protecting spacer is disposed between the plural semiconductor chips and the heat spread plate, that resin is filled around the semiconductor chips sandwiched between the heat spread plate and the wiring board, and that the semiconductor chips are interconnected through the resin.

(22) The present invention, in a still further aspect thereof, resides in a semiconductor module having a structure wherein a plurality of bare or packaged semiconductor chips are mounted on a wiring board while circuit-formed sides thereof face up, the semiconductor chips and the wiring board are metal wire-bonded to each other, and a single heat spread plate is disposed on the circuit-formed sides of the plural semiconductor chips, characterized in that a metal wire protecting spacer is disposed between the wiring board and the heat spread plate, that resin is filled around the semiconductor chips sandwiched between the heat spread plate and the wiring board, and that the semiconductor chips are interconnected through the resin.

(23) The semiconductor module according to the present invention is obtained by mounting a plurality of semiconductor chips on a wiring board, disposing a heat spread plate, and pouring resin between the wiring board and the heat spread plate. As a resin pouring method there may be adopted a method wherein resin lumps or pellets are put respectively on upper surfaces of semiconductor chips a heat spread plate is then put thereon, then pressing plates are disposed outside both the wiring board and the heat spread plate and pressing is performed under heating, allowing the resin to melt or soften and flow and thereby allowing it to be filled around the semiconductor chips. There also may be adopted a method wherein a wiring board a heat spread plate and semiconductor chips are placed in a mold and a resin is poured into the mold by a transfer press molding. There also may be adopted a method wherein resin lumps or pellets are placed between semiconductor chips mounted on a wiring board and a heat spread plate, which are then placed together into an autoclave, followed by heating to melt or soften and flow the resin, allowing the resin to be filled around the semiconductor chips.

(24) The present invention in still further aspects will become more apparent from working examples thereof to be described later.
(25) The semiconductor chips used in the present invention are bare or packaged semiconductor chips. Bare chips are each formed with a circuit on one side thereof and are each provided with input-output terminals, designated pads, terminals, electrodes, or electrode terminals. In many cases, the input-output terminals are formed on a circuit-formed side of each semiconductor chip.

(26) As an example of a packaged semiconductor chip there is mentioned CSP. An example of CSP is described in Japanese Patent Laid-open No. Hei 9-321084.

(27) According to the CSP described therein, a wiring tape is disposed through a stress buffer layer on a circuit-formed side of a chip and is electrically connected to pads on the chip which connected portions are sealed using a resin, with metal bumps being formed on the wiring tape. The CSP of this structure is suitable for use in the present invention. Examples of such packaged semiconductor chips include SOJ (Small Outline J-lead package). TSOP (Thin Small Outline Package), and TCP (Tape Carrier Package), in addition to CSP, all of which are employable in the present invention.

(28) In the present specification, the term "semiconductor chip" cover both bare chips and packaged semiconductor chips unless otherwise mentioned. Further, the term mounting" as referred to herein refers, in a narrow sense, to a technique of mounting a semiconductor chip on a wiring board and connecting it to the board electrically, while in a broad sense, it refers to the technique plus a subsequent heat spread plate bonding technique or resin pouring technique. The "metal bump" as referred to herein corresponds to the bump electrode referred to in the prior art.

(29) In the semiconductor module according to the present invention, since semiconductor chips are interconnected through a resin, even if a stress is exerted on any of the chips, it is dispersed in all directions through the resin. Thus, there is no fear of the chips and the heat spread plate being cracked. Besides, since the bonding between the semiconductor chips and the heat spread plate is produced by the resin, the heat spread plate is not likely to tilt, unlike the case where a heat

transfer part is used. Further, in the semiconductor module having a structure wherein metal bumps are formed between semiconductor chips and a wiring board, since resin is filled between the chips and the wiring board, the thermal conductivity from the chips to the wiring board is improved and the metal bumps are difficult to be oxidized. The resin also serves to protect the chips and prevent bending of the module.

(30) A semiconductor device having a structure in which a semiconductor chip is sandwiched between a substrate and a heat spread plate and a resin is molded around the chip, is disclosed in Japanese Patent Laid-open Nos. Hei 7-11278 and Hei 9-17827. But, the assembly of a multi-chip module is not described therein.

As to the grounds of rejection under section 103, see MPEP § 2113.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,679,697,678,685,723,777,778,698 385/89,88 361/777,748, 324/761,754,769,755,765,758,158.1 716/5 365/201 439/502	3/31/05
Other Documentation: foreign patents and literature in 257/686,679,697,678,685,723,777,778,698 385/89,88 361/777,748, 324/761,754,769,755,765,758,158.1 716/5 365/201 439/502	3/31/05
Electronic data base(s): U.S. Patents EAST	3/31/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
3/31/05